REMARKS

Reconsideration of this application as preliminarily amended is respectfully requested.

Claims 34-41 are rejected under 35 U.S.C. 112, first paragraph. The Examiner states that

> Claims 34-41 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 34 describes a "discard enable signal input." The specification mentions the possibility of discarding at page 18, lines 3-8; page 20, lines 15-18; page 24, lines 9-14; page 31, lines 3-6; page 32, lines 6-7; and page 32, lines 15-16. But there is not mention of either a discard enable signal or an input (e.g., a port) for such a signal. Claims 35-41 depend on claim 34 and are therefore similarly rejected.

(p. 4, Office Action 10/24/00). Applicants have amended Claim 34 to eliminate the reference to a discard enable signal input, as requested by the Examiner. No new matter has been added by the amendment. As Claims 35-41 were rejected as being dependent on Claim 34, the clarification of Claim 34 extends to Claims 35-41.

Claims 1-3, 22, 25-32, 42-45, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. of 5, 940,368 of Takamichi et al. (Takamichi) in view of U.S. Patent No. 5,406,554 of Parry (Parry). The Examiner states that

> With regard to claims 1, 3, 42, and 43, Takamichi et al. discloses an apparatus comprising at least one bidirectional FIFO unit, wherein each such bidirectional FIFO unit comprises a first and second unidirectional FIFO buffer (Fig. 6; column 6, lines 28-32; cell buffer pairs 51—55, 7-8, and 61-65). Takamichi et al. fails to disclose an invention for which the buffer word size is programmable. Parry teaches a FIFO buffer that is useful for ATM applications and whose word size can be programmed by either

using more that one FIFO or varying the width of the input data bus (Fig. 3; column 13, lines 23-39). Because the word size can be programmed, the cell size can be programmed (see the specification at page 30, line 27 to page 31, line 3). It would have been obvious to one of ordinary skill in the art to modify the invention of Takamichi et al. so that the word size of each of the FIFO buffers is programmable, as in Parry, because such a modification allows the invention to be used on a larger number of servers because servers vary in the word size they handle.

(p. 4, Office Action 07/16/01).

Applicants respectfully submit that Claims 1 and 42 are not obvious under Takamichi in view of Parry. Claim 1 as amended claims the limitation: "wherein a fixed-length transmission unit size of the first and second unidirectional FIFO buffers comprises <u>a software programmable parameter changeable by the user</u> <u>without the need to change existing hardware.</u>" (Claim 1)(emphasis added). Claim 42 as amended claims the limitation: "wherein the bi-directional FIFO unit comprises a first and second unidirectional FIFO buffer having <u>a software</u> <u>programmable fixed-length transmission unit size changeable by the user</u> <u>without the need to change existing hardware.</u>" (Claim 42)(emphasis added).

It is submitted Takamichi does not teach or suggest a combination with Parry, nor does Parry teach or suggest a combination with Takamichi. It is further submitted that combining Takamichi with Parry is impermissible hindsight based on applicant's own disclosure. Even when combined, neither Takamichi nor Parry disclose the fixed-length transmission unit size of the first and second unidirectional FIFO buffers comprises a software programmable parameter changeable by the user without the need to change existing hardware. Takamichi never contained any such limitation. Parry discloses that

With reference now to FIG. 3, an expanded width FIFO 76 is shown. Expanded width FIFO 76 incorporates two FIFOs 10 as previously described with respect to FIG. 1. Further, with respect to expanded width

FIFO 76 as illustrated in FIG. 3, like structure to that above-described with respect to FIG. 1 is like numbered, and the foregoing description thereof shall suffice herefor.

In the example shown in FIG. 3, two input data buses 14 may be combined to a width of 18 bits or to any multiples of 8 or 9 as may be required. Utilizing the dual write and read enable signals of FIFO 10, along with separate count down clocks, data from an 8 or 9 bit bus can be stored in whatever width desired, and then re-interleaved back into an 8 or 9 bit format on output data buses 64 to allow the use of slower FIFO's 10 on fast data buses.

(Parry, Col. 13, lines 23-39). Parry discloses physically varying the size of the FIFO memory capacity and the cell bus bandwidth.

Given that claims 2-33 depend from claim 1 and claims 43-49 depend from claim 42, and the above limitation fails to appear in the other cited references, applicants submit that claims 2-33 and 43-49 are not obvious under 35 U.S.C. §103(a) by the references cited by the Examiner for at least these reasons.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections have been overcome.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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1.   (Amended)   An apparatus for controlling fixed-length transmission unit traffic in a switch platform, the apparatus comprising at least one bi-directional first-in-first-out (FIFO) unit, wherein each bi-directional FIFO unit comprises a first and a second unidirectional FIFO buffer, wherein a fixed-length transmission unit size of the first and second unidirectional FIFO buffers [is programmable] comprises a software programmable parameter changeable by the user without the need to change existing hardware.

3.   (Amended)   The apparatus of claim 1, wherein a word size of the first and second unidirectional FIFO buffers is [programmable] a software programmable parameter.

34.   (Amended)   A network switch platform comprising:

at least one service module;

at least one fixed-length transmission unit bus controller coupled among the at least one service module and at least one switch;

at least one bi-directional first-in-first-out (FIFO) unit located in the at least one service module and the at least one fixed-length transmission unit bus controller, wherein each bi-directional FIFO unit comprises a first and a second unidirectional FIFO buffer each capable of discarding an invalid fixed-length transmission unit, wherein a fixed-length transmission unit size of the first and second unidirectional FIFO buffers [is programmable] comprises a software programmable parameter changeable by the user without the need to change existing hardware; and

at least one diagnostic interface, wherein the at least one diagnostic interface supports a non-destructive read of the at least one bi-directional FIFO unit while at least one fixed-length transmission unit is being written to and read from the at least one bi-directional FIFO unit[; and

at least one discard enable signal input to the at least one bidirectional FIFO unit, wherein at least on invalid fixed-length transmission unit can be discarded from the at least on bi-directional FIFO unit upon receiving a discard enable signal via the at least one discard enable signal input].

39.   (Amended)   The network switch of claim 34, wherein a word size of the first and second unidirectional FIFO buffers is [programmable] a software programmable parameter.

42.   (Amended)   A method for controlling fixed-length transmission unit traffic in a switch platform, the method comprising the step of transferring at least one fixed-length transmission unit among a plurality of ports having a plurality of bandwidths using a bi-directional first-in-first-out (FIFO) unit, wherein the bi-directional FIFO unit comprises a first and second unidirectional FIFO buffer having a software programmable fixed-length transmission unit size changeable by the user without the need to change existing hardware.